

CLAIMS

- 1 1. A system comprising:
2 a plurality of cores;
3 a first test access port controller coupled to at least one core;
4 a second test access port controller coupled to at least one core; and
5 a select pin to control the first and second test access port controller to support a plurality
6 of system modes of operation.
- 1 2. The system of claim 1 further comprising:
2 a first multiplexer coupled to the first test access port controller, the second test access
3 port controller, and to a first plurality of Joint Test Action Group (JTAG) signals; and
4 a second multiplexer coupled to the second test access port controller, a second plurality
5 of Joint Test Action Group signals and to a plurality of pins.
6
- 1 3. The system of claim 1 wherein the system is a system on a chip (SoC).
2
- 1 4. The system of claim 1 wherein the plurality of system modes of operation is at least two
2 of a debug mode, an emulation mode, or a test of at least one of the plurality of cores.
3
- 1 5. The system of claim 2 wherein the second multiplexer forwards the plurality of JTAG
2 signals to the second test access port controller for either a debug mode of operation or an
3 emulation mode of operation.

1 6. The system of claim 2 wherein the first multiplexer forwards the plurality of JTAG
2 signals to the first test access port controller for either a debug mode of operation, or an
3 emulation mode of operation, or to test one of the cores.

1 7. The system of claim 2 wherein the second multiplexer does not forward the plurality of
2 JTAG signals to the second test access port controller for the system mode of operation to test
3 one of the plurality of cores, and the plurality of pins coupled to the second multiplexer are
4 utilized for other functional purposes for the system mode of operation to test one of the plurality
5 of cores.

1 8. A method for controlling test access port controllers comprising:
2 generating a select signal;
3 selecting either a first test access port controller or second access port controller for a first
4 mode of operation in response to the select signal; and
5 selecting both the first test access port controller and second access port controller for a
6 second mode of operation in response to the select signal.

1 9. The method of claim 8 further comprising:
2 multiplexing between a plurality of Joint Test Action Group signals and a plurality of
3 pins.

1 10. The method of claim 8 wherein the select signal comprises either a single pin or a
2 combination of two pins.

1 11. The method of claim 8 wherein the first mode of operation is testing a single core.

12. The method of claim 8 wherein the second mode of operation is either a debug mode of operation or an emulation mode of operation.

13. The method of claim 9 wherein the multiplexing comprises:
forwarding the Joint Test Action Group signals in response to the second mode of operation; and
forwarding the pins in response to the first mode of operation for other functional uses.

14. A system comprising:
a plurality of cores;
a first multiplexer coupled to a first test access port controller and to at least one core;
a second multiplexer coupled to a second test access port controller and to at least one core;
a first pin to control the first multiplexer; and
a second pin to control the second multiplexer.

15. The system of claim 14 further comprising:
a plurality of Joint Test Action Group signals coupled to the first and second multiplexer;
and
a plurality of pins coupled to the second multiplexer.

16. The system of claim 14 wherein the first pin is to select a core for a test mode of operation.

1 17. The system of claim 14 wherein the second pin is to select either one of a functional
2 mode of operation, or a debug mode of operation, or an emulation mode of operation.

1 18. The system of claim 15 wherein the second multiplexer forwards the plurality of JTAG
2 signals to the second test access port controller for either a debug mode of operation or an
3 emulation mode of operation.

1 19. The system of claim 15 wherein the first multiplexer forwards the plurality of JTAG
2 signals to the first test access port controller for either a debug mode of operation, or an
3 emulation mode of operation, or to test one of the cores.

1 20. The system of claim 14 wherein the second multiplexer does not forward the plurality of
2 JTAG signals to the second test access port controller for a mode of operation to test one of the
3 plurality of cores, and the plurality of pins coupled to the second multiplexer are utilized for
4 other functional purposes for the system mode of operation to test one of the plurality of cores.